REMARKS

As an initial matter, Applicants note that the Office Action of August 10, 2004, is incomplete since Claims 10 and 53-57 have not been considered. In a telephone conversation with Examiner Norris on January 3, 2005, Examiner Norris indicated that these claims had not been considered due to an oversight. Thus, Applicants respectfully request that Claims 10 and 53-57 now be considered on the merits. Applicants note that the next Office Action, if necessary, must be Non-final unless Claims 10 and 53-57 are allowed.

Turning to the response, Claims 9-13, 22-26, 32, 37, 38 and 42-52 are pending in the application. Claims 9-13 and 48-51 are allowed. Claim 44 is objected to under 37 C.F.R. § 1.75(c). Claims 43 and 46 are objected to as being dependent on a rejected base claim. Claim 32 is rejected under 35 U.S.C. § 112, second paragraph. Claim 22-26, 32, 37-38, 40-42 and 52 are rejected under 35 U.S.C. § 102.

Claims 22, 23, 24, 25 32 and 37 are amended herein. The specification is also amended herein.

In Claim 22, at line 3, the phrase "at least" is deleted. The phrase "and an electroplated film" is inserted at line 3 after the phrase "an electroless plated film." Also, the phrase "is formed on a surface of said roughened surface and" is inserted after the phrase "said electroless plated film." Support for the amendment can be found, for example, in Example 3, Figs. 12(c)-(d) and 13(a)-(d).

In Claim 23, at line 3, the phrase "at least" is deleted. The phrase "and an electroplated film" is inserted at line 3 after the phrase "an electroless plated film." Also, the phrase "a surface

of" is inserted after the phrase "complementary to." Support for the amendment can be found, for example, in Example 3, Figs. 12(c)-(d) and 13(a)-(d).

In Claim 24, at line 2, the phrase "by a build-up process" is inserted after "built thereon. At line 6, the phrase "said lower-layer conductor circuit has a roughened surface," is inserted after "wherein." At line 7, the phrase "and an electroplated film" is inserted after "an electroless plated film." At line 9, "and" is deleted. At line 13, after the term "layer," the phrase "and said lower-layer conductor circuit and said electroless plated film formed on the bottom of said via hole are connected through said roughened surface of said lower-layer conductor circuit" is inserted. Support for this amendment can be found, for example, in Example 3, Figs. 11(b), 12 (a)-(d) and 13 (a)-(d).

In Claim 25, the preamble is changed to read "the printed circuit board according to Claim 22." Support for this amendment can be found, for example, on page 49, lines 16-26.

In Claim 32, at line 2, the phrase "on both sides" has been inserted in place of "a" before the term "conductor." Also, throughout Claim 32, the term "circuit" which appears numerous times after the term "conductor" has been deleted and replaced with "circuits," and the phrase "each of" has been inserted where indicated before the "said conductor circuits." Also, the phrase "and the same as the thickness of said conductor layer on said interlayer resin insulating layer" has been deleted. Support for this amendment can be found, for example, in Example 4 and Fig. 23.

In Claim 37, at line 2, the phrase "and on both sides thereof," has been deleted and replaced with "having on both sides conductor circuits conductor circuits and, over each set of

said conductor circuits, a." Also, "wiring layers" has been deleted and replaced with "wiring layer." At line 5, the phrase "is a copper-clad laminate, and" is inserted before "is provided." At line 6, the phrase said conductor circuits comprise a copper foil of said copper-clad laminate and a plated film, and" is inserted before "said via holes." Support for the amendment can be found in Example 15 and Figs. 32 to 37.

Claim 44 has been amended to depend from Claims 40-42.

In the specification, the paragraph bridging pages 78 and 79 has been amended to correct the description of Figures 2(a) to 2(e). The correction of these errors does not introduce new matter and is supported by the use of the correct terminology on page 79, lines 14-16, and Figures 2(c) to 2(e).

Response to Objection to Claim 44

Claim 44 is objected to under 37 C.F.R. § 1.75(c) as allegedly being in improper form.

As indicated above, Claim is amended to be multiply dependent on Claims 40-42. Since none of Claims 40-42 is a multiple dependent claim, it is respectfully submitted that the objection to Claim 44 be withdrawn.

Response to the Claims Rejection under 35 U.S.C. § 112, second paragraph

Claim 32 is rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctively claim the subject matter which applicant regards as the invention.

It was asserted that claim 32 does not clearly set forth the metes and bounds of the patent protection desired because the claim allegedly recites a broad range along with a narrow range

that falls within the broad range. Specifically, it is asserted that claim recites the broad range "the thickness of said conductor circuit is not greater that 10μm than the thickness of said conductor layer" and the narrow range "the thickness of said conductor circuit is substantially the same as the thickness of said conductor layer on said interlayer resin insulating layer."

Applicants respectfully submit that Claim 32, as amended, complies with the provisions of 35 U.S.C. § 112, second paragraph. As indicated above, the recitation "the thickness of said conductor circuit is substantially the same as the thickness of said conductor layer on said interlayer resin insulating layer" has been deleted. Thus, Applicants submit that the rejection of Claim 32 under § 112, second paragraph, should be reconsidered and withdrawn.

Response to the Claim Rejections under 35 U.S.C. § 102

Claims 22, 23 and 52 are rejected under 35 U.S.C. 102 (b) as allegedly being anticipated by U.S. Patent No. 4,642,163 to Greschner et al. ("Greschner").

Claims 24, 32, 37, 38, 40-42 and 45 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,258,094 to Furui et al. ("Furui").

Claims 25 and 26 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,021,296 to Suzuki et al. ("Suzuki").

1. Response to the Rejection of Claims 22, 23 and 52

Applicants respectfully submit that Greschner fails to teach or suggest the presently claimed invention.

Claim 22 recites "[a] printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, thereon, a conductor circuit comprising an electroless

plated film and an electroplated film, wherein said electroless plated film is formed on a surface of said roughened surface and has a stress of 0 to +10 kg/mm^2."

Applicants note that in the circuit board of Claim 22, the plated film of the printed circuit board "adheres intimately" to the substrate (*see* page 34, lines 24-26). Furthermore, the plated film "hardly peels off from the substrate" after a reliability test under high temperature, high humidity and high pressure conditions (*see* page 34, lines 24-26, Table 3).

Applicants submit that the circuit board of Greschner is quite different from the presently claimed circuit board.

Greschner discloses printed circuit board comprising a substrate 1 with recesses 4, a sputtered-on copper layer 6, and an electroless-deposited copper 7. *See* Figure 1F.

Applicants concede that printed circuit board of Greschner is roughly analogous to the printed circuit board of the present invention in that a conductor circuit is formed on the surface of a roughened surface.

Applicants assert, however, that the copper layer 6 of Greschner is formed on the roughened surface by sputtering. In contrast, the electroless plated film of the present invention is formed on the roughened surface. Furthermore, even though Greschner discloses the adhesion strength of a metallic layer (in the order of 1000 n/m) with respect to a non-conductive surface (*see* col. 2, lines 41-45), Greschner is silent with respect to the stress of the electroless plated film.

Applicants note that the present invention addresses the problems associated with ensuring the adhesion strength between a roughened surface and a circuit using an electroless

plated film. For instance, an electroless plated film may suffer stress during formation, and as a result, the film tends to peel off the surface.

Typically, an electroless plated film is formed via the reaction between an oxidant and a reductant. In this reaction, hydrogen gas is generated. This hydrogen gas is absorbed during the formation of the electroless plated film resulting in an electroless plated film with an internal stress.

When this internal stress is a compressive stress, the electroless plated film tends to expand and easily peel off from the resin insulating layer (*see* page 4, lines 26-28). In contrast, when the internal stress is a large tensile stress, the electroless plated film tends to shrink and peel off the roughened surface of the resin insulating layer.

Thus, either type of stress can cause an electroless plated film being formed on a roughened surface tends to peel off of the resin insulating layer.

Applicants note that since the copper layer 6 of Greschner on the roughened surface is formed by sputtering, the constitution of the conductor circuit of Greschner is different from that of the present invention. Furthermore, the sputtered layer 6 does not have the above-mentioned problem, *i.e.* stress caused by a hydrogen uptake and a drop of adhesion strength caused by said stress. Also, Greschner does not teach the stress of the copper layers 6 and 7.

Greschner does teach a metallic layer with an adhesion strength of 1000 n/m. This adhesion strength is equivalent to 1.0 kg/cm (*see* col. 2, lines 41 to 45 of Greschner). In contrast, the present invention teaches a metallic layer having a peel strength of 1.0 to 1.3 kg/cm (page 48, line 4 in the specification). Applicants submit that even if an electroless plated film suffering

from stress is formed on a roughened surface, a higher adhesion strength can be ensured, without a help of an expensive sputtering apparatus, so long as the stress is adjusted to within a range of 0 to +10 kg/mm^2.

As noted in the present specification, the stress can be adjusted to a range of 0 to +10 kg/mm^2 by using an electroless plating solution containing tartaric acid or its salt. Such an electroless plating solution can reduce the amount of hydrogen uptake (*see* page 34, lines 19 to 21).

In view of the foregoing, Applicants submit that Greschner fails to teach the printed circuit board of Claim 22. Also, since Greschner does not disclose problems arising from stress, one of ordinary skill in the art would not have been motivated to attain the printed circuit board according to the present invention.

Accordingly, it is submitted that the rejection of Claim 22 (as well as the rejection of Claim 52) should be reconsidered and withdrawn.

Turning to the rejection of Claim 23, the printed circuit board recited therein comprises "a resin insulating substrate board formed with a roughened surface and, built thereon by semi-additive process, a conductor circuit comprising an electroless plated film and an electroplated film, wherein said roughened surface comprises convex areas and concave areas, and said electroless plated film is complementary to a surface of said roughened surface with said electroless plated film in convex areas of said roughened surface being relatively greater in thickness than said electroless plated film in concave areas of said roughened surface."

Applicants note that the circuit of the printed circuit board according to Claim 23 has good insulation reliability (*see* page 37, lines 16-18).

As discussed above, the circuit board of Greschner is roughly analogous to the printed circuit board of the present invention in that a conductor circuit is formed on a surface of a roughened surface. However, the copper layer 6 of Greschner is formed on the roughened surface by sputtering, whereas the electroless plated film of the present invention is formed on a roughened surface.

The circuit board of Greschner further differs from the present invention in that the copper layer 6 of Greschner has almost the same thickness in the recess 4 and on top of the resin 2 (*see* Fig. 1F of Greschner). The electroless-deposited copper 7 in the recess 4 has a thickness even greater than the thickness on the top of the resin 2. In contrast, in the present invention, the electroless plated film in the convex areas of the roughened surface is greater in thickness than the electroless plated film in the concave areas.

In addition, Applicants submit that Greschner does not teach forming a separated circuit. In the present invention, a semi-additive process is employed to form the circuit wherein a separated circuit is formed by etching the electroless plated metal layer beneath the plating resist (*see* page 37, lines 7-12).

The etching operation of the present invention is easier when the thickness of the electroless plated metal layer is relatively thinner in the concave areas as compared with the convex areas (*see* page 37, lines 12-14). When the electroless plated metal layer in the concave areas is thick, the plated metal layer cannot be fully removed since the etching solution does not

spread well into the concave areas. Thus, the plated metal layer may remain between the circuits and the reliability of the insulation is reduced. Therefore, since the conductor circuit of the present invention is formed by semi-additive process, the electroless plated metal layer in the convex areas is thicker than in the concave areas.

Applicants submit that such a difference in thickness is not present in Greschner since Greschner does not teach to form a separated circuit.

Accordingly, Applicants submit that rejection of Claim 23 should be reconsidered and withdrawn.

2. Response to the Rejection of Claims 24, 32, 37, 38, 40-42 and 45

Applicants respectfully submit that Claims 24, 32, 37, 38, 40-42 and 45 are not anticipated by Furui.

With respect to Claim 24, the printed circuit board recited therein comprises "a substrate board formed with a lower-layer conductor circuit -and, built thereon by a build-up process, an upper-layer conductor circuit through the intermediary of an interlayer resin insulating layer, with said upper-layer conductor circuit and said lower-layer conductor circuit being interconnected by via holes, wherein said lower-layer conductor circuit has a roughened surface, said upper-layer conductor circuit comprises an electroless plated film and an electroplated film, said interlayer resin insulating layer is provided with a roughened surface, with said electroless plated film being complementary to said roughened surface, said interlayer resin insulating layer and said via holes are provided with the same electroless plated film, with said electroless plated film formed on the bottoms of said via holes having a thickness equal to 50 to 100% of the

thickness of said electroless plated film formed on said interlayer resin insulating layer, and said lower-layer conductor circuit and said electroless plated film formed on the bottom of said via hole are connected through said roughened surface of said lower-layer conductor circuit."

Applicants submit that when the openings for via holes are as fine as 80 μm or less in diameter, a sufficiently thick plated metal film can be formed on the hole bottoms (*see* page 37, lines 7 to 12). Thus, the peeling of the plated film can be prevented even though the printed circuit board is prepared by a build-up process.

Furui discloses a multilayer printed wiring board comprising a copper-laminated plate 10 with a copper foil layer 25, an electroless plated conductive layer 65, an insulating resin 9 with a roughened surface, an electroless plated conductive layer 64 and a photoviahole 42. The electroless plated conductive layer 64 is formed on both the insulating resin 9 and the photoviahole 42. The thickness of the electroless plated conductive layer 64 at the bottom of the photoviahole 42 is 12-18 μm.

Applicants submit that the following features of Furui are roughly analogous to those of printed circuit board of Claim 24: the plate 10 with the conductor layers 25 and 65, which is analogous to the substrate board formed with a lower-layer conductor circuit; the insulating resin 9 with a roughened surface, which is analogous to the interlayer resin insulating layer; the electroless plated conductive layer 64, which is analogous to the upper-layer conductor circuit; and the photoviahole 42, which is analogous to the via hole.

Accordingly, the multilayer printed wiring board according to Furui is roughly analogous to the printed circuit board of the present invention in that an upper-layer conductor circuit is

built on the substrate board wherein a lower-layer conductor circuit with an interlayer resin insulating layer is interposed between the upper-layer conductor circuit and the substrate board. In addition, the interlayer resin insulating layer is provided with a roughened surface and the upper-layer conductor circuit and the lower-layer conductor circuit is interconnected by a via hole. It is also noted that the interlayer resin insulating layer and the via hole are provided with the same electroless plated film and the electroless plated film is complementary to the roughened surface of the interlayer resin insulating layer. It is further noted that the electroless plated film formed on the bottoms of the via holes has a thickness equal to 50 to 100% of the thickness of the electroless plated film formed on the interlayer resin insulating layer.

Applicants assert, however, that the multilayer printed wiring board of Furui is prepared by application of heat and pressure (*see* col. 5, lines 42 to 44). In contrast, the printed circuit board of the present invention is formed by a build-up process. Further, the conductor layer 65 of Furui does not have a roughened surface, whereas the lower-layer conductor circuit of the present invention has a roughened surface.

Applicants further assert that the electroless plated conductive layer 64 of Furui does not comprise an electroplated film. On the other hand, the upper-layer conductor circuit of the present invention comprises an electroless plated film and an electroplated film.

Thus, it is respectfully submitted that the printed circuit board of the present invention has a different structure from the multilayer printed wiring board of Furui.

Applicants further note that in the present invention the lower-layer conductor circuit has a roughened surface, so that the contact area of the lower-layer conductor circuit with the

electroless plated film in the via hole increases considerably. This results in an increase of adhesive strength.

Also, the electroless plated film bites into the irregularities of the roughened surface of the lower-layer conductor circuit. This suppresses the power of the electroless plated film in the via hole which tends to expand or shrink to release stress. As a result, the electroless plated film in the via hole is inhibited from peeling off from the lower-layer conductor circuit.

In contrast, in the circuit board of Furui, the layers are integrated by pressing under heat and pressure. In the process, the hydrogen in the electroless plated conductive layer 64 is released. Applicants submit that it is less likely that the electroless plated conductive layer 64 peels off from the conductive layer 65 compared to a layer wherein the hydrogen is not released.

It is noted, however, that in Furui the contact area is not as large as that of the present invention since the contact surface is flat. Furthermore, the electroless plated conductive layer 64 does not bite into the irregularities of the roughened surface of the conductive layer 65. Therefore, it is still more likely that the electroless plated conductive layer of Furui peels off when subjected to a thermal cycle compared to the electroless plated conductive layer of the present invention. Applicants reiterate that the roughened surface of the lower-layer conductor circuit in the present invention inhibits the electroless plated film in the via hole from peeling off.

In view of the foregoing, it is respectfully submitted that the rejection of Claim 24 should be reconsidered and withdrawn.

Turning to the rejection of Claim 32, the multilayer printed circuit board recited therein comprises "a core board having on both sides conductor circuits and, over each of said conductor circuits, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes, wherein said core board comprises a copper-clad laminate, each of said conductor circuits comprises a copper foil of said copper-clad laminate and a plated metal layer, the thickness of each of said conductor circuits is not greater by more than 10 μm than the thickness of said conductor layer on said interlayer resin insulating layer."

Applicants note that the circuit board of Claim 32 allows for an impedance alignment to be easily attained between the conductor circuit on the core board and the conductor layer on the interlayer resin insulating layer (*see* page 55, lines 4 to 9). In addition, the size and the thickness of the multilayer printed circuit board can be reduced.

For the sake of convenience, Applicants point out that the following features of Furui's circuit board are roughly analogous to those of the multilayer printed circuit board of Claim 32: the plate 10 with the conductor layers 25 and 65, which is analogous to the core board (comprising a copper-clad laminate) formed with a conductor circuit; the insulating resin 9 and the electroless plated conductive layer 64, which are analogous to the buildup wiring layer; the photoviahole 42, which is analogous to the via hole.

Accordingly, the multilayer printed wiring board according to Furui is roughly analogous to the multilayer printed circuit board of the present invention: a buildup wiring layer is formed

over a conductor circuit on a core board; a core board comprises a copper-clad laminate; and conductor layers are interconnected by via holes.

Further, the thickness of the conductor layer 25 is 12 to 35 μm (*see* col. 4, lines 29 to 30) and the thickness of the conductor layer 65 is 12 to 18 μm (*see* col. 4, lines 35 to 38). Thus, the sum of which is 24 to 53 μm. The sum is 6 to 41 μm larger than the thickness of the electroless plated conductive layer 64, which is 12 to 18μm (*see* col. 5, lines 11 to 14). Applicants note that this feature is analogous to the present invention in that the thickness of the conductor circuit on the core board is not 10 μm greater than the thickness of the conductor layer on the interlayer resin insulating layer.

Applicants note, however, that Furui teaches forming the buildup wiring layer on one side of the core board. In the present invention, the buildup wiring layers are formed on both sides of the core board in the center of the multilayer printed circuit board. When the buildup wiring layers are formed on both sides of the core board, it is possible to obtain a printed circuit board with one core board, and, as a result, reduce the thickness of the printed circuit board.

In addition to an easily attained impedance alignment and a reduced thickness of the multilayer printed circuit board, the wiring length is shortened and the loop inductance is reduced. Applicants note that these effects result in improved high-frequency characteristics.

Applicants therefore submit that since Furui does not teach the structure or the effect of the present invention, Claim 32 is neither anticipated nor rendered obvious over Furui.

Turning to the rejection of Claim 37, the circuit board recited in Claim 37 comprises "a core board having on both sides conductor circuits and, over each of said conductor circuits, a

buildup wiring layer comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein said conductor layers are interconnected by via holes, wherein said core board is a copper-clad laminate, and is provided with plated-through holes, said conductor circuits comprise a copper foil of said copper-clad laminate and a plated film, and said via holes are formed immediately over said plated-through holes in the manner of plugging the through holes in said plated-through holes and are interconnected with said plated-through holes."

Applicants note that the multilayer printed circuit board of Claim 37 has an improved high-frequency characteristic. Applicants further note that the region immediately over the plated-through hole may function as an internal layer pad, and, as a result, it is possible to eliminate a dead space. Thus, the layout density of plated-through holes in the multilayer core board can be increased (*see* page 69, lines 12 to 19). Also, the distance between a plated-through hole electrically connected to the supply terminal of an IC and a plated-through hole electrically connected to the ground terminal of an IC can be shortened. Accordingly, the mutual inductance is reduced and, as a result, the loop inductance is reduced. Furthermore, since circuits connecting plated-through holes with via holes are not necessary, the space for forming circuits is increased in the buildup wiring layer. This structure allows for the number of buildup wiring layers to be reduced, the length of the wiring to be shortened, the loop inductance to be reduced, and the impedance to be reduced.

In other words, since via holes are formed immediately over plated-through holes, the distance between the plated-through holes in the core board is shortened, the connection between the via hole and the plated-through hole is minimized, and the number of buildup wiring layers

can be reduced. Accordingly, the wiring length is shortened. Applicants submit that these conditions improve the high-frequency characteristics of the multilayer printed circuit board of the present invention.

Applicants respectfully submit that Furui fails to teach the circuit board of Claim 37. For the sake of convenience, Applicants note that the following features of Furui are roughly analogous to those of the multilayer printed circuit board of Claim 37: the prepreg layer 52, which is analogous to the core board; the insulating resin 9 and the conductive layers 62 and 65, which are analogous to the buildup wiring layer; and the conductive paste layer 5, which is analogous to the plated-through holes.

Accordingly, the multilayer printed wiring board according to Furui is roughly analogous to the multilayer printed circuit board of the present invention in that the buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer are formed on both sides of a core board, and the board is provided with a plated-through hole.

Applicants note however, that the prepreg layer 52 does not comprise a copper-clad laminate. Furthermore, the conductive layers 63 and 64 comprise a plated layer, as opposed to a copper foil of a copper-clad laminate. Therefore, the conductive layers 63 and 64 do not correspond to the conductor circuits of the present invention.

Applicants submit that even if the conductive layers 63 and 64 of Furui were considered to correspond to the conductor circuits of the present invention, the via holes 41 would not be formed immediately over the conductive paste layer 5 in the manner of plugging the conductive paste layer 5.

Applicants further submit that Furui is silent about a core board that comprises a copper-clad laminate, a conductor circuit comprising a copper foil of a copper-clad laminate and a plated film, and a via hole formed immediately over a plated-through hole in the manner of plugging the through hole in the plated-through hole. Thus, Applicants assert that the multilayer printed circuit board of Claim 37 is not anticipated by Furui.

With respect to rejection of Claims 40-42, Applicants submit that Furui fails to teach or suggest the circuit boards recited in Claims 40-42.

Applicants note that the multilayer printed circuit boards recited in Claims 40-42 have improved high-frequency characteristics. Applicants further note that the region immediately over the plated-through hole may function as an internal layer pad, and, thus, eliminates dead space. As a result, the layout density of via holes and circuits in the buildup wiring layers is increased. In addition, the number of buildup wiring layers is reduced, and the wiring length is shortened. Furthermore, since at least two via holes (lower-layer via holes and upper-layer via holes) are present immediately over plated-through holes, the length of a wiring comprising the plated-through holes and the via holes is large.

This structure allows a wiring, which comprises a plated-through hole electrically connected to the supply terminal of an IC and via holes formed immediately over the plated-through hole, and a neighboring wiring, which comprises a plated-through hole electrically connected to the ground terminal of an IC and via holes formed immediately over the plated-through hole, to extend parallel to each other for a long distance. This parallel wiring allows for the mutual inductance and the loop inductance to be reduced.

Applicants note that the following features of Furui are roughly analogous to those of the multilayer printed circuit board of Claims 40-42: the prepreg layer 52, which is analogous to the core board; the insulating resin 9 and the conductive layers 62, 63, 64 and 65, which are analogous to the buildup wiring layer; the conductive paste layer 5, which is analogous to the plated-through holes; and the photoviahole 42 connecting the conductive layers 62 and 63, or the conductive layers 64 and 65, which is analogous to the lower-layer via hole. Applicants additionally note that the photoviahole 42 is disposed immediately over the conductive paste layer 5.

However, Furui is silent about an upper-layer via hole. Furui does not teach to dispose a via hole immediately over the photoviahole 42. Accordingly, the multilayer printed circuit board according to the present invention is different in constitution from the multilayer printed wiring board according to Furui.

As discussed above, in the present invention, the number of buildup wiring layers is reduced, and the wiring length is shortened. In addition, the impedance is reduced. These characteristics allow for improved high-frequency characteristics.

Thus, in view of these reasons, Applicants submit the circuit board of Claims 40-42 is neither taught, suggested nor rendered obvious by Furui. Accordingly, Applicants submit that the rejection of Claims 40-42 should be reconsidered and withdrawn.

3. Response to the Rejection of Claims 25 and 26

Applicants respectfully submit that Suzuki fails to teach, suggest or render obvious the subject matter recited in Claims 25 and 26.

As an initial matter, Applicants respectfully submit that Claims 25 and 26 cannot be anticipated by Suzuki since Suzuki fails to anticipate Claim 22, the claim from which Claims 25 and 26 depend. Thus, for this reason, it is submitted that the rejection of Claims 25 and 26 should be reconsidered and withdrawn.

Turning to the merits of the rejection, as indicated above, Claim 25 recites "[a] printed circuit board according to claim 22, wherein said electroless plated film is a copper film, and comprises at least one metal species selected from the group consisting of nickel, iron and cobalt."

With this structure, the uptake of hydrogen is suppressed and the compressive stress is reduced. As a result, the electroless plated film has a good adhesion to the resin insulating layer. In addition, with this structure the metals form alloys with copper to increase the hardness of the plated metal film, which allows the adhesion to the resin insulating layer to be further improved (*see* page 39, lines 13-19).

As shown in Fig. 1D of Suzuki, the circuit board of Suzuki comprises a resin substrate 2 and a copper wiring 3 formed from a copper foil 1. The surface of the copper wiring 3 is roughened, and a copper oxide-reduced layer 4 is formed thereon. A nickel plating layer is then deposited on the copper oxide-reduced layer 4 (*see* col. 5, lines 43-44). Next, a plurality of the metal-clad laminate boards are laminated with the substrates 2 in between (*see* Fig. ID). After forming throughholes, a multi-layered circuit board is obtained (*see* col. 5, line 55, to col. 6, line 8). Suzuki further teaches that it is preferable to deposit 5×10^{-7} to 1×10^{-4} g/cm^2 of nickel and/or cobalt on the copper oxide-reduced layer (*see* col. 3, lines 54-56).

Applicants note that Suzuki also teaches a process wherein one side of a copper foil 1 is etched, a copper oxide-reduced layer 4 is formed thereon, and a nickel layer is deposited on the copper oxide-reduced layer 4. *See* Example 13. A resin substrate 2 and the pair of copper foils 1 are hot pressed while facing the deposited nickel layer to the resin substrate 2 (*see* Fig. 3A). Then, an electroless copper plating layer 6 is formed (*see* Fig. 3B) to finally obtain a circuit board.

Applicants note that the circuit board of Suzuki is somewhat similar the invention of Claim 25 in that the resin substrate 2 has a roughened surface.

The circuit of Suzuki does not comprise an electroless plated conductor circuit 6 which is formed on a roughened surface of the resin substrate 2. Furthermore, Suzuki does not recognize the problems associated with stress in the conductor circuit 6. In addition, Suzuki fails to teach the presence of an electroplated film.

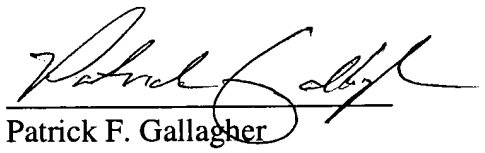
Suzuki also fails to teach that the electroless copper plating layer 6 comprises at least one metal species selected from the group consisting of nickel, iron and cobalt. Furthermore, Suzuki fails to teach that the electroless plated layer has an increased hardness and adhesion.
Applicants assert that Suzuki fails to teach the structure of the present invention. Suzuki also fails to suggest the effect of the present invention. Thus, it is submitted that the rejection of Claims 40-42 should be reconsidered and withdrawn.

In view of the above, reconsideration and allowance of this application, including Claims 9-13, 22-26, 32, 37, 38, 40-42, 45 and 52, are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved

through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Patrick F. Gallagher
Registration No. 54,109

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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23373
CUSTOMER NUMBER

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